Automatic Synthesis of A 2.1GHz SiGe Low Noise Amplifier

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Abstract **A 2.1GHz low noise amplifier in a 0.5μm 47GHz SiGe BiCMOS process was synthesized and sent to fabrication. The circuit was synthesized to simultaneously meet multiple design specifications including noise figure, gain, power, impedance match, intermodulation, compression, stability with a state-of-art simulation-based circuit synthesis tool. The synthesis setup took about two days, and the synthesis run took about 2 hours on a pool of 10 networked SUN workstations. Noise figure of 1.2dB, power gain of 16dB, IIP3 of -6dB, S11 of less than -15dB, were achieved with 3.7mA bias current at 2.5V power supply. Data generated during synthesis was processed to show design trade-offs among competing performance goals. The trade-off between optimum noise match and input impedance match is discussed.**

I. Introduction

The design of a radio-frequency circuit involves numerous trade-offs between competing specifications including power, noise, gain, linearity, stability, impedance match among others. A typical design, such as a front-end low noise amplifier, may take months for a designer with years of experience. On the other hand, rapid evolution of wireless standards and fierce market competition demand minimal design effort and time-to-market with no compromise of product quality. Traditional labor-intensive manual design methodologies can no longer meet the challenge. Automatic RF/analog circuit synthesis is emerging as a promising approach to reduce design cycle time and increase productivity[1][2]. After decades of research, practical analog synthesis tools have recently become available[3].

With relatively few devices, but many trade-offs, radio frequency circuits are good candidates for automatic synthesis. Fewer devices mean fewer design variables and thus a smaller search space for synthesis. A typical RF circuit function block has only a couple up to a dozen transistors and about the same number of passive components, such as inductors, capacitors and resistors. Independent design variables may be even fewer considering device matching constraints. Design problems with such scale are well suited for current synthesis tools.

II. RF/Analog Synthesis Flow

In this paper, we used a simulation-based synthesis tool [3] which requires minimal preparatory effort compared to knowledge-based tools. The flow diagram is shown in Fig. 1. Commercial simulators, such as Spectre RF (used for simulations for this paper), Eldo RF, Star-Hspice and ADS†, or proprietary simulators, such as TIspice, can be easily interfaced with the synthesis engine to guarantee industrial accuracy. Unlike most optimization/tuning tools, the synthesis tool does not require a starting point for design parameters. Required inputs are circuit topology, circuit design variables, and performance specifications. As in a traditional manual design flow, the simulation environment must be setup before synthesis. The simulation environment consists of a few testbenches for the evaluation of circuit performance. The synthesis engine synthesizes and evaluates 10^3 to 10^4 candidate designs with efficient searching algorithm and produces several designs which meet or exceed all the specifications if there exit solutions. In addition to the final designs, the large body of data generated during synthesis is available to the designers for design space exploration. The large simulation load is distributed to parallel networked computers to leverage the ever-increasing computing power of modern workstations.

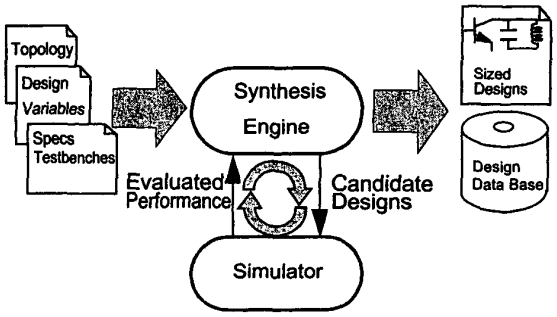

Fig. 1. RF/Analog synthesis flow diagram

III. Synthesis Setup For The LNA Circuit

A single stage common emitter gain stage with emitter inductive degeneration is chosen for the low noise ampli-

† Spectre, Eldo, Star-Hspice and ADS are trademarks of Cadence Design Systems, Mentor Graphics, Avant! and Agilent respectively.

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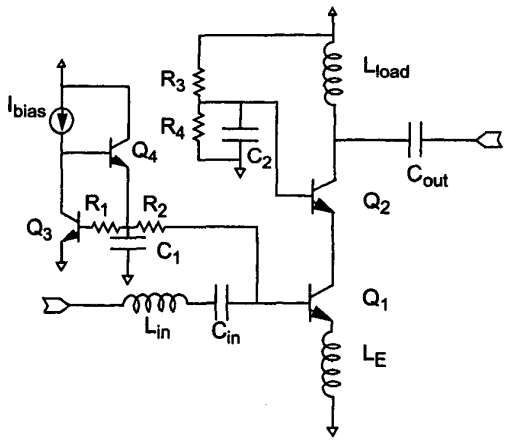

Fig. 2. Simplified low noise amplifier schematic.

fier as shown in Fig. 2. A cascode transistor is used for better isolation and ease of impedance match. High Q bond wire inductors are chosen for input inductor L_{in} and degeneration inductor L_E for lower noise and flexibility of impedance match during test. The load inductance L_{load} is implemented as an on-chip spiral inductor. Since only about 20 inductor models with discrete inductance are provided by the foundry, L_{load} is not a fully designable component. One of the foundry designed and modeled on-chip inductors is selected. For the input NPN transistor Q_1, the multiplier is chosen to be fixed and the emitter length l_{E1} is picked as a design variable. The multiplier and emitter length of cascode transistor Q_2 (m_2, l_{E2}) are both chosen as design variables. Parasitic capacitance at Q_2 collector is resonant with the fixed L_{load} and forms an L-match with C_{out} to achieve output impedance match. The collector current is designed to be $6*I_{bias}$. All told, there are 7 independent design variables, namely, l_{E1}, l_{E2}, m_2, L_{in}, L_E, C_{out}, I_{bias}. The ranges and increment steps of the design variables are set by rough hand calculations considering the design rules of the process. Even though the synthesis tool can accommodate large ranges, a set of reasonable ranges prevents an unnecessarily large search space and therefore speeds up the synthesis. As listed in Table I, the ranges are loose enough for a designer to estimate in negligible time.

Three test benches are set up to evaluate candidate circuits during synthesis: one for four S-parameters, noise figure and DC power consumption, one for IIP3, and the last one for large signal 1dB compression point. There is a total of 9 basic performance goals: noise figure, gain(S21), S11, S12, S22, stability K-factor, IIP3, 1dB compression and power consumption. To synthesize toward a noise match, two more goals are added: Γ_{min}, which is the reflection coefficient with minimum noise figure and δNF, which is the difference between 50Ω noise figure and minimum noise figure. Performance specifications are listed in Table II together with the final synthesis results.

TABLE I
SYNTHESIS SETUP OF DESIGN VARIABLES

Design Variables	From	To	Step
l_{E1} (μm)	5	15	1
l_{E2} (μm)	5	15	1
m_2	3	12	1
L_{in} (nH)	1	5	0.25
L_E (nH)	0.5	1.5	0.1
C_{out} (pF)	0.1	1	0.1
I_{bias} (mA)	0.1	1	0.1

IV. SYNTHESIS RESULTS

The setup time for the synthesis is about 2 days which is comparable to the setup time for simulation in a traditional design flow. The synthesis takes approximately 2 hours on a pool of 10 SUN workstations. Most of the synthesis time is due to the time-consuming periodic-steady-state simulations for the IIP3 and 1dB compression computation. When synthesis is complete, instead of providing only one final design, the synthesis tool provides a collection of good designs all of which meet performance goals. In addition, numerous candidate design points that are visited during synthesis process, some of which may have not met one or more of the design goals, are stored and available for design exploration through data mining. To perform data mining, a set of design points are selected according to a set of performance specification criteria to rule out non-sense design points. Then trade-offs between any two performance specifications or design variables can be plotted to give valuable design insight.

A. *Noise match vs. input impedance match*

As reported in [4], optimum noise-matched and input impedance matched low noise amplifier can be designed in four steps: first the minimum noise current density $J_{c\text{-}opt}$ is found at the specified frequency; secondly the emitter length (l_{E1}) of the input transistor is adjusted so that optimum noise figure source resistance (R_{sopt}) equals 50Ω at

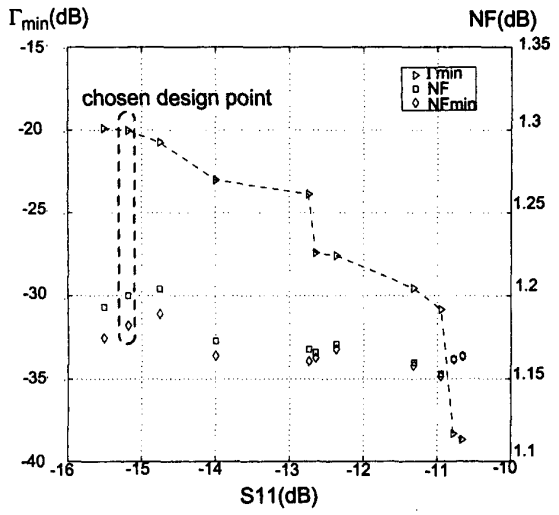

Fig. 3. Trade-off between input reflection S11 and reflection coefficient with minimum noise figure Γ_{min}, corresponding NF and NFmin are also shown.

minimum noise current density; then the emitter degeneration inductor L_E is added to match the real part of the input impedance to 50Ω without changing the R_{sopt}; finally the input matching inductor L_{in} is inserted to transform the imaginary part of both input impedance and optimum NF source impedance to zero at the same time. In the end, simultaneous noise match and input impedance match is reportedly achieved.

Sequential design/optimization approach as stated above tackles an optimization problem with multiple goals by decomposing it into a few sub-problems and solving them one by one. Since design variables and goals are tightly coupled, such one-variable-at-a-time approach always requires many design iterations to meet all the goals. In contrast, we simultaneously synthesize all involved design variables, e.g., L_E, L_{in}, emitter length(l_{E1}), and I_{bias}, to minimize noise figure, input reflection (S11) and reflection coefficient with minimum noise figure(Γ_{min}) at the same time.

Synthesis results are post-processed through data mining and are shown in Fig. 3. Design points with Γ_{min} lower than -15dB and S11 lower than -10dB are selected to generate the plot. A trade-off between noise match (Γ_{min}) and input impedance match (S11) is evident from the plot. It shows that for designs with Γ_{min} lower than -20dB, S11 can hardly be lower than -15dB. After taking a close look at the designs, we find that even though the real parts of optimum NF noise impedance (R_{sopt}) and input impedance (R_{in}) are matched to 50Ω, their imaginary parts, X_{sopt} and X_{in}, can not be matched to zero simultaneously. Several factors contribute to this result. First, the optimum NF source reactance (X_{sopt}) of a PNP transistor, which is inductive, is not exactly in conjugate with the input reactance(X_{in}), which is capacitive, as assumed in [4]. The same situation exists for a MOSFET and results in the fundamental trade-off between noise and impedance match[5]. Secondly, after connecting in the emitter degeneration inductor, X_{sopt} is reduced more than X_{in} is increased. Consequently, X_{in} and X_{sopt} can not be transformed to zero at the same time. In addition, parasitics introduced by bond pads make simultaneous noise and impedance match more difficult. Nevertheless, with good S11 (< -15dB), excellent noise match (Γ_{min} < -20dB), which corresponds to less than 0.02dB NF degradation, can be achieved. In Fig. 3, achieved noise figure and minimum noise figure vs. S11 are also plotted.

B. Other trade-off Analyses

Many trade-off plots can be obtained after synthesis. As an example, Fig. 4. shows the effects of L_E on gain and IIP3. Higher L_E results in higher IIP3 but lower gain, while lower L_E results in higher gain but lower IIP3. Moreover, a close inspection of the graph reveals that L_E has a dominant effect on gain, which can be deduced from the tight distribution of design points along the line, while there are other factors significantly affecting IIP3 besides L_E, which is evident from the relatively wide spread of design points.

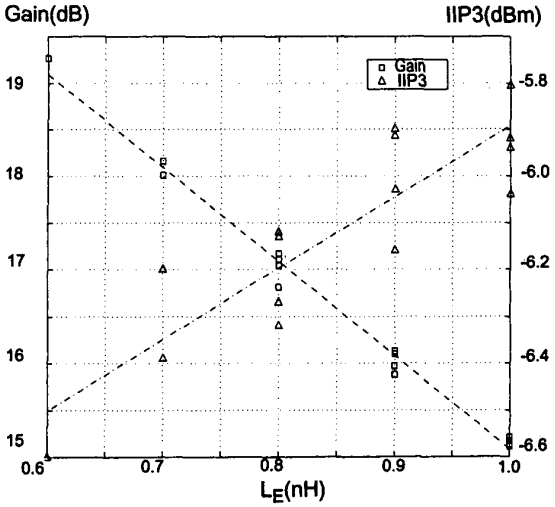

Fig. 4. Effects of L_E on gain and IIP3, Design points have different spread along two lines.

TABLE II
LNA SYNTHESIS SPECIFICATIONS AND RESULTS

Performance	Specifications	Results
S21	>15dB	16dB
NF	<1.5dB	1.2dB
Input-IP3	>-10dBm	-6dBm
Input-P1dB	>-20dBm	-15dBm
S11	<-15dB	-15dB
S22	<-20dB	-21dB
S12	<-30dB	-39dB
K_factor	>1	4
Γ_{min}	<-15dB	-20dB
δNF	<0.02dB	0.015dB
ICC	<5mA	3.7mA
VCC	-	2.5V
Frequency	-	2.1GHz

V. IMPLEMENTATION

One of the best design points was selected for the final implementation. The input NPN size is 0.5μm x 9μm x 12, and L_E is 0.9nH. Layout was performed manually with the aid of an automatic analog layout tool[6]. The layout was extracted and verified by simulation. The LNA takes about 600μm by 600μm excluding bond pads, as shown in Fig. 5. The simulated performances are listed in Table II. The design was sent out to be implemented in the IBM 0.5μm SiGe BiCMOS process with an NPN f_t of 47GHz[7].

VI. CONCLUSION

A 2.1GHz SiGe low noise amplifier was synthesized and layed out for fabrication. We have demonstrated that a simulation-based synthesis tool can successfully synthesize block-level radio-frequency circuits, such as an LNA, with minimal preparatory effort and affordable runtime. Compared with traditional manual design, the new design methodology achieves an order of magnitude saving in design time with designs rivaling expert manual designs. Furthermore, the vast design database generated during synthesis can be processed to explore trade-offs among design variables and performance specifications. As an example, the trade-off between noise match and input impedance match of the SiGe bipolar transistor was examined.

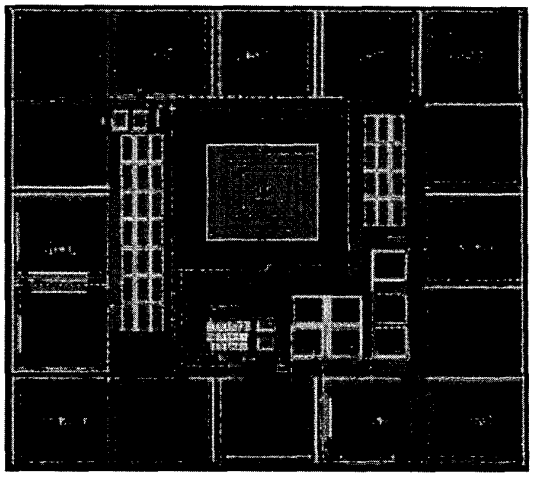

Fig. 5. Layout of the low noise amplifier.

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